United States Court of Appeals for the Federal Circuit

01-1449, -1583, -1604, -1641, 02-1174, -1192

RAMBUS INC.,

Plaintiff-Appellant,
v.

INFINEON TECHNOLOGIES AG,
INFINEON TECHNOLOGIES NORTH AMERICA CORP.,
and INFINEON TECHNOLOGIES HOLDING NORTH AMERICA INC.,

Defendants-Cross Appellants

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Appealed from: United States District Court for the Eastern District of Virginia

Judge Robert E. Payne

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DECIDED: January 29, 2003

Before RADER, BRYSON, and PROST, Circuit Judges.

Opinion for the court filed by Circuit Judge RADER. Dissenting opinion filed by Circuit Judge PROST.

RADER, Circuit Judge.

During trial, the United States District Court for the Eastern District of Virginia granted judgment as a matter of law (JMOL) and held that Infineon Technologies AG, Infineon Technologies North America Corp., and Infineon Technologies Holding North America Inc. (collectively Infineon) did not infringe Rambus Inc.'s patents. The jury later found Rambus liable for fraud associated with standard-setting activities on two computer memory technologies. On post-trial JMOL motions, the district court set aside a verdict of fraud on one of the memory technologies, but permitted the fraud verdict to stand on the other technology. The court then issued an injunction against Rambus and awarded Infineon attorney fees.

Because the district court erred in its claim construction, this court vacates the grant of JMOL of noninfringement and remands for consideration under the revised claim construction. Additionally, because substantial evidence does not support the implicit jury finding that Rambus breached the relevant disclosure duty during its participation in the standards committee, this court reverses the denial of JMOL that let the fraud verdict stand. Based on the record evidence, the district court properly set aside the fraud verdict on the remaining technology. These holdings render the injunction moot and require this court to vacate and remand the attorney fees award for reconsideration in light of this opinion. The record evidence supports the district court's grant of JMOL Accordingly, this court vacates-in-part, reverses-in-part, affirms-in-part, and remands.

I.

Rambus develops and licenses memory technologies to companies that manufacture semiconductor memory devices. Rambus does not manufacture any memory devices itself, but relies instead on licensing its patent portfolio for revenue. In April

1990, Rambus filed U.S. Patent Application Serial No. 07/510,898 ('898 application) with claims directed to a computer memory technology known as dynamic random access memory (DRAM). The United States Patent and Trademark Office (PTO) determined that the '898 application covered multiple independent inventions. The PTO issued an eleven-way restriction requirement requiring Rambus to elect one invention to pursue in the '898 application. In response, Rambus filed numerous divisional and continuation applications based on the original '898 application -- at least thirty-one of which have issued. Many of these patents claim aspects of a memory technology known as Rambus DRAM (RDRAM). In April 1991, Rambus filed a patent application under the Patent Cooperation Treaty (WIPO application) claiming priority to the '898 application.

In December 1991, Rambus attended a Joint Electron Devices Engineering Council (JEDEC) meeting as a guest. Rambus officially joined JEDEC in February 1992. JEDEC is a standard-setting body associated with the Electronic Industries Association (EIA).[1] JEDEC member companies participate on various committees to develop standards for semiconductor technologies. Committee JC-42.3 drafts standards for random access memory (RAM), a common component in computers, printers, and other electronic devices. JEDEC meetings are open meetings, but nonmembers must receive an invitation to attend. Minutes of the JEDEC meetings and copies of the published JEDEC standards are available to members and nonmembers alike. Both JEDEC and EIA have a written patent policy encouraging the adoption of standards free of patented items or processes. At least by 1993, the EIA/JEDEC patent policy required members to disclose patents and patent applications "related to" the standardization work of the committees.

During Rambus's membership on committee JC-42.3, JEDEC adopted a standard for synchronous dynamic random access memory (SDRAM). SDRAM increases the speed at which a central processing unit (CPU) can read or write memory by synchronizing itself with the CPU's clock speed. JEDEC incorporated four technologies into its SDRAM standard that are relevant to this case: programmable CAS latency, programmable burst length, externally supplied reference voltage, and two-bank designs. JEDEC adopted and published its SDRAM standard in early 1993. Since 1993, JEDEC has published several revisions of the standard.

Rambus attended its last JEDEC meeting in December 1995, and officially withdrew from JEDEC in June 1996. In December 1996, JEDEC began work on a standard for double data rate-SDRAM (DDR-SDRAM), the successor to SDRAM. DDR-SDRAM doubles the transfer rate between the CPU and memory device by supporting data transfers on both the rising and falling edge of each clock cycle. The JEDEC DDR-SDRAM standard ultimately incorporated four technologies that had been discussed in general before Rambus's withdrawal in 1996. Those technologies include: source-synchronous clocking, low-voltage swing signaling, dual clock edge, and on-chip phase locked loop/delay locked loop (PLL/DLL). JEDEC adopted and published the DDR-SDRAM standard in 2000.

In September 1993, Rambus disclosed its first issued RDRAM patent, U.S. Patent No. 5,243,703 ('703 patent), a divisional of the '898 application, to JEDEC during a committee meeting. As a divisional, the written description of the '703 patent is substantially identical to that of the '898 application. At that same meeting, another

JEDEC member also disclosed Rambus's WIPO application to the committee. Rambus did not disclose any patent applications to JEDEC. After leaving JEDEC Rambus filed more divisional and continuation applications based on the '898 application. Four of the patents that issued from those applications are at issue in the present case, namely U.S. Patent Nos. 5,954,804 ('804 patent), 5,953,263 ('263 patent), 6,034,918 ('918 patent), and 6,032,214 ('214 patent). Rambus filed the applications that ripened into these four patents between February 1997 and February 1999. Again, the written description of each of these patents is substantially identical to that of the '703 patent and the '898 application. The first of these four patents issued in 1999.

In late 2000, Rambus sued Infineon, a manufacturer of semiconductor memory devices (including SDRAM and DDR-SDRAM) and a member of JEDEC, for infringement of the patents-in-suit. Rambus alleged infringement of fifty-seven claims in the four patents. Infineon counterclaimed for fraud under Virginia state law. Infineon alleged that Rambus committed fraud by not disclosing to JEDEC its patents and patent applications "related to" the SDRAM and DDR-SDRAM standards. After construing the claims, the district court granted JMOL of noninfringement in favor of Infineon under Rule 50(a) of the Federal Rules of Civil Procedure. Fed. R. Civ. P. 50(a); Rambus, Inc. v. Infineon Techs. AG, No. 3:00CV524, slip op. at 1-2 (E.D. Va. May 2, 2001); Rambus, Inc. v. Infineon Techs. AG, No. 3:00cv524, slip op. at 1-2 (E.D. Va. May 30, 2001). Infineon's fraud counterclaims were tried to a jury. The jury found that Rambus committed fraud during SDRAM and DDR-SDRAM standardization. Rambus moved for JMOL of no fraud on both the SDRAM and DDR-SDRAM verdicts. Alternatively, Rambus requested a new trial. The district court denied JMOL on the SDRAM fraud verdict. The court granted JMOL on the DDR-SDRAM fraud verdict, holding that substantial evidence did not support the jury's verdict because Rambus left JEDEC before work officially began on the DDR-SDRAM standard. Rambus, Inc. v. Infineon Techs. AG, 164 F. Supp. 2d 743, 767 (E.D. Va. 2001). The district court also denied Rambus's request for a new trial on the SDRAM verdict, but conditionally granted a new trial on DDR-SDRAM should this court reverse that grant of JMOL. The court issued an injunction against Rambus, Rambus, Inc. v. Infineon Techs. AG, No. 3:00cv524, slip op. at 35 (E.D. Va. Aug. 9, 2001), and awarded Infineon attorney fees, Rambus, Inc. v. Infineon Techs. AG, 155 F. Supp. 2d 668, 691 (E.D. Va. 2001).

Both parties appealed to this court, which has jurisdiction under 28 U.S.C. § 1295(a)(1) (2000). Rambus appeals the denial of JMOL and the denial of a new trial on the SDRAM verdict. Additionally, Rambus appeals the court's claim construction, the grant of JMOL of noninfringement, the injunction on domestic suits, and the attorney fees award. Infineon cross-appeals the grant of JMOL on the DDR-SDRAM verdict and the court's refusal to enjoin Rambus's pending foreign suits against Infineon.

II.

This court reviews a grant or denial of JMOL without deference by reapplying the JMOL standard. Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448, 1454, 46 USPQ2d 1169, 1172 (Fed. Cir. 1998) (en banc); Dennis v. Columbia Colleton Med. Ctr., Inc., 290 F.3d 639, 644-45 (4th Cir. 2002); Fed. R. Civ. P. 50(a)(1). For matters submitted

to and decided by a jury, this court will affirm a grant or reverse a denial of JMOL only "if the jury's factual findings are not supported by substantial evidence or if the legal conclusions implied from the jury's verdict cannot in law be supported by those findings." Cybor Corp., 138 F.3d at 1454; Havird Oil Co. v. Marathon Oil Co., 149 F.3d 283, 289 (4th Cir. 1998). This court draws all reasonable inferences in favor of the prevailing party without substituting its view of conflicting evidence for that of the jury. SIBIA Neurosciences, Inc. v. Cadus Pharmaceutical Corp., 225 F.3d 1349, 1355, 55 USPQ2d 1927, 1930 (Fed. Cir. 2000);Dennis, 290 F.3d at 645.

Before deciding whether an accused device infringes asserted claims, a court must first construe the claim language to determine the meaning and scope of the claims. Cybor Corp., 138 F.3d at 1454. This court reviews claim construction without deference. Id. at 1456.

This court reviews state law causes of action under the applicable state law for matters not committed to this court's exclusive jurisdiction. Univ. of W. Va. Bd. of Trustees v. Vanvoorhies, 278 F.3d 1288, 1296, 61 USPQ2d 1449, 1453 (Fed. Cir. 2002); Hunter Douglas, Inc. v. Harmonic Design, Inc., 153 F.3d 1318, 1338, 47 USPQ2d 1769, 1783 (Fed. Cir. 1998). Thus, this court applies Virginia commonwealth law to the fraud actions.

Although Virginia has not stated clearly whether detecting the existence of a duty to disclose is a question of law or fact,[2] the district court considered the issue a question of fact. As such, the jury had the responsibility to interpret and construe the written EIA/JEDEC patent policy. On appeal, neither party contests the district court's submission of this issue to the jury. Therefore, this court will analyze the existence of a duty to disclose as a question of fact.[3]

A district court may award a prevailing party attorney fees under 35 U.S.C. § 285 in exceptional cases. This court reviews without deference the district court's application of the proper legal standard under § 285. Brasseler, U.S.A. I, L.P. v. Stryker Sales Corp., 267 F.3d 1370, 1378, 60 USPQ2d 1482, 1487 (Fed. Cir. 2001); cf. Reactive Metals & Alloys Corp. v. ESM, Inc., 769 F.2d 1578, 1582, 226 USPQ 821, 824 (Fed. Cir. 1985). In reviewing a § 285 award, this court reviews underlying factual findings, including whether a case is exceptional, for clear error and underlying legal conclusions without deference. Molins PLC v. Textron, Inc., 48 F.3d 1172, 1186, 33 USPQ2d 1823, 1833 (Fed. Cir. 1995). If the case is found to be exceptional, the district court enjoys broad discretion to make an award, a determination that this court reviews for an abuse of discretion. Brasseler, 267 F.3d at 1379. If the factual or legal underpinnings of the award partially are reversed, this court may vacate the award and remand for further evaluation by the district court. Molins, 48 F.3d at 1186.

III. Claim Construction and Infringement

After construing the asserted claims, the district court granted JMOL in favor of Infineon, holding that Infineon did not infringe the claims as construed. On appeal, Rambus contests the construction of five terms in the four patents-in-suit, namely: "integrated circuit device," "read request," "write request," 'transaction request," and "bus." The parties agree that, with one exception, the terms have the same meaning in each claim at issue. The only exception is the term "integrated circuit

device," which Infineon argues has a different meaning in the '804 patent because of representations made to the PTO during prosecution of that patent.

Patent claim language defines the scope of the invention. SRI Int'l v. Matsushita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc). As a general rule, claim language carries the meaning of the words in their normal usage in the field of the invention. Toro Co. v. White Consol. Indus., 199 F.3d 1295, 1299, 53 USPQ2d 1065, 1067 (Fed. Cir. 1999). In other words, a claim term means "what one of ordinary skill in the art at the time of the invention would have understood the term to mean." Markman v. Westview Instruments, Inc., 52 F.3d 967, 986, 34 USPQ2d 1321, 1335 (Fed. Cir. 1995) (en banc), aff'd 517 U.S. 370 (1996). Nevertheless, inventors may act as their own lexicographers and use the specification to supply implicitly or explicitly new meanings for claim terms. Id. at 980; Bell Atl. Network Servs., Inc. v. Covad Communications Group, Inc., 262 F.3d 1258, 1268, 59 USPQ2d 1865, 1870 (Fed. Cir. 2001) ("[A] claim term may be clearly redefined without an explicit statement of redefinition."); Scimed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc., 242 F.3d 1337, 1344, 58 USPQ2d 1059, 1065 (Fed. Cir. 2001). Thus, to help determine the proper construction of a patent claim, a construing court consults the written description and the prosecution history. Digital Biometrics, Inc. v. Identix, Inc., 149 F.3d 1335, 1344, 47 USPQ2d 1418, 1424 (Fed. Cir. 1998).

While claims often receive their interpretative context from the specification and the prosecution history, courts may not read limitations into the claims. Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1186, 48 USPQ2d 1001, 1005 (Fed. Cir. 1998). "This court has repeatedly and clearly held that it will not read unstated limitations into claim language." N. Telecom Ltd. v. Samsung Elecs. Co., 215 F.3d 1281, 1290, 55 USPQ2d 1065, 1072 (Fed. Cir. 2000); see also Renishaw PLC v. Marposs Societa' per Azioni, 158 F.3d 1243, 1248, 48 USPQ2d 1117, 1120 (Fed. Cir. 1998); Markman, 52 F.3d at 981.

A. Integrated Circuit Device

The district court construed "integrated circuit device" in claim 26 of the '804 patent to include a device identification register, interface circuitry, and comparison circuitry.

Claim 26 recites:

26. An integrated circuit device having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises:

a first internal register to store a value which is representative of a number of clock cycles to transpire before the integrated circuit device responds to a read request;

delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals; and

interface circuitry, coupled to the external bus to receive a read request, the interface circuitry includes a plurality of output drivers, coupled to the external bus,

to output data on the external bus in response to the internal clock signal, synchronously with respect to the first and second external clock signals and in accordance with the value stored in the first internal register.

'804 patent, col. 28, ll. 1-21. Nothing in the claim language indicates that "integrated circuit device" necessarily includes a device identification register, interface circuitry, and comparison circuitry. The terms "comparison circuitry" and "device identification register" do not appear anywhere in the text of claim 26.[4] "Comparison circuitry" is different from the "delay locked loop circuitry" limitation recited in claim 26. Likewise, a "device identification register" is different from the limitation "first internal register to store a value which is representative of a number of clock cycles." Thus, the claim does not require comparison circuitry or a device identification register. The district court's construction did not merely clarify or construe the actual words of the claim. Without any claim language addressing comparison circuitry or a device identification register, the court's construction reads into the claim two new limitations not required by the claim language. See N. Telecom, 215 F.3d at 1290.

The district court erred by placing too much emphasis on a single introductory comment in the prosecution history of the '804 patent. This comment appeared in the prosecution history after the examiner rejected the pending claims in light of U.S. Patent No. 4,458,357. Responding to the rejection, the patentee submitted twenty-six new claims, four of which were independent claims. In accompanying remarks, the patentee stated:

These newly submitted claims are directed to a memory device (or an integrated circuit having memory) having (1) aninternal register for storing an identification value, (2) interface circuitry to receive a request on an external bus, and (3) comparison circuitry to determine whether the identification information in the request corresponds to the identification value in the internal register – wherein when the identification information corresponds to the identification value, the memory device responds to the request.

While the first three independent claims (issued claims 1, 15, and 23) recited, with some modifications, the three limitations listed above, the fourth independent claim (issued claim 26) recited only one of the above listed limitations. Specifically, claim 26, the claim at issue here, includes only the "interface circuitry" limitation. Claim 26, however, contains two other limitations not listed above: an internal register to store a value representative of a number of clock cycles and delay locked loop circuitry.

The prosecution history statement introduces in general terms the new claims. In this sense, the statement properly introduces three features that appear in some of the claims. This general introductory statement, however, is not correct in suggesting that these features appear in each of the new claims. This incorrect statement in the prosecution history does not govern the meaning of the claims. Therefore, consistent with Intervet America, Inc. v. Kee-Vet Laboratories, Inc., 887 F.2d 1050, 12 USPQ2d 1474 (Fed. Cir. 1989), the imprecise statement in

the prosecution history does not limit claim 26. The claim language itself controls the bounds of the claim, not a facially inaccurate remark during prosecution. The patent at issue in Intervet involved a vaccine for a poultry disease. Id. at 1051. In that case the examiner rejected the pending claims because they were not limited to a single vaccination. The examiner said that a single vaccination limitation would distinguish the invention over the prior art. Id. at 1053-54. The prosecuting attorney amended three of the claims to recite "single administration," but did not so amend the remaining claims. Id. at 1054. In accompanying remarks, the attorney inaccurately described all the claims as "restricted to a single vaccination scheme." Id. After this erroneous remark, the examiner had two interviews with the attorney and made two examiner's amendments before allowing the claims. Id. Reviewing this prosecution history, this court in Intervet held that the claims control over a loose remark in the course of prosecution:

When it comes to the question of which should control, an erroneous remark by an attorney in the course of prosecution of an application or the claims of the patent as finally worded and issued by the [PTO] as an official grant, we think the law allows for no choice. The claims themselves control. . . . [I]t is not for the courts to say that they contain limitations which are not in them.

Id. The Intervet court thus did not restrict all of the claims to a single vaccination. Id.; see also Hockerson-Halberstadt v. Avia Group Int'l, 222 F.3d 951, 957, 55 USPQ2d 1487, 1491 (Fed. Cir. 2000).

The present case parallels Intervet. Here, claim 26 does not contain all the limitations found in claims 1, 15, and 23 of the '804 patent. The prosecuting attorney's incorrect description of the four new claims does not govern over the language of those claims. Moreover, in this case, the examiner made an examiner's amendment and amended each of the claims -- including claim 26 -- after this untrue remark by the prosecuting attorney. In this context, a reasonable competitor would not rely on an untrue statement in the prosecution history over the express terms of the claims. In the present case, like Intervet, this court perceives no justification for reading unstated limitations into claim 26.

The term "integrated circuit device," as used in claim 26, instead receives its ordinary meaning to one of skill in this art as a "circuit constructed on a single monolithic substrate, commonly called a 'chip.'" See Rambus, Inc. v. Infineon Techs. AG, No. 3:00cv524, slip op. at 70 (E.D. Va. March 15, 2001) (Rambus argues for this construction.); cf. The New IEEE Standard Dictionary of Electrical and Electronic Terms 662 (5th ed. 1993); IBM Dictionary of Computing 347 (10th ed. 1994); see also Texas Digital Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193, 1202, 64 USPQ2d 1812, 1818 (Fed. Cir. 2002).

B. Read Request

The district court construed "read request" to mean "a series of bits transmitted over the bus that contain multiplexed address and control information needed to request a read of data from a memory device." The court similarly construed "write request" and "transaction request" by replacing the language "needed to request a read of data from a memory device" with "needed to request a

write of data from a memory device" and "needed to perform a transaction over the bus with a memory device."

Claim 18 of the '918 patent is representative of the claims reciting a "read request:"

18. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:

receiving an external clock signal;

receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request;

receiving a first request from the bus controller; and

outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal.

'918 patent, col. 26, ll. 13-27 (emphases added). The relevant claim language thus recites only that data is output onto a bus in response to a "read request."

Both parties agree that the term "read request" has no unambiguous ordinary meaning to one of skill in the art. Infineon argues that because the claims contemplate a response to a "read request," the "read request" must contain all information necessary to perform the requested read. Thus, Infineon argues that the "read request" must include both address and control information. Rambus agrees that in order to actually perform a read the device must be given address and control information. Rambus asserts, however, that such address and control information is part of the "request packet," not the "read request." Rambus argues that "read request" refers only to an instruction to the memory device to perform a read action. According to Rambus, the "read request" is one component of the "request packet" -- comprising the first four bits of the packet. Figure 4 of the '918 patent illustrates a "request packet:"

As shown above, the "request packet" has multiple fields, including an AccessType field, Address fields, and a BlockSize field. Rambus contends that the four-bit AccessType field contains the "read request." The first bit instructs the memory device to perform a read; the next three bits tell the device what type of read to perform (e.g., page read, normal access read, etc.).

The district court interpreted the claim language requiring a response to a "read request" to mean that the "read request" must include address and control information. To the contrary, the claim language itself shows the fallacy of holding that outputting data in response to a "read request" necessarily implies that the read request must contain all information necessary for a memory device to respond. Claim 18 recites receiving a "block size" that defines an amount of data to

be output onto a bus in response to a read request. By specifying the "block size" as separate from the "read request," claim 18 indicates that the block size is not part of the read request. Nevertheless, block size, which tells the device how much data to read, is necessary to permit the device to respond to a read request.[5] Thus, even though the device needs a block size to respond, such block size is not part of the read request. See '918 patent, col. 24, l. 58–col. 25, l. 3 (Claim 1 recites providing a "block size" to the memory device in one limitation and issuing a "read request" to the memory device in another limitation.).

In addition, the district court's interpretation of "read request" conflicts with other passages of the specification. While the memory device must respond to a read request, the specification indicates that the address and control information is part of the request packet -- not the read request. In other words, the specification does not use read request and request packet interchangeably. Rather, it shows a difference between a read request and a request packet. Each reference to address and control information consistently indicates that such information is a part of the request packet, which the specification defines as "a contiguous series of bytes containing address and control information." '918 patent, col. 8, l. 59–col. 9, l. 4; see also col. 9, ll. 24–43; col. 6, ll. 61–62 (defining request packet as "a sequence of bytes comprising address and control information"); col. 9, ll. 11–13 (request packet has control information). Other than in the abstract and the claims, the term "read request" appears only twice in the specification. See id., col. 9, l. 2 & col. 12, ll. 33-35. Neither reference to "read request" suggests the presence of address and control information. The specification merely indicates that the "read request" requests data from a memory device and specifies what type of read (e.g., page mode, normal mode, etc.) to perform. See id., col. 9, l. 39-col. 10, l. 39; col. 8, l. 66-col. 9, l.3 & Figure 4.

Moreover, the dependent claims demonstrate that a read request is distinct from a request packet. Dependent claims 27 and 28, which depend from claim 18, recite:

27. The method of claim 18 wherein the first block size information and the first read request are included in a request packet.

28. The method of claim 27 wherein the first block size information and the first read request are included in the same request packet.

id., col. 27, ll. 6-11. Although one of ordinary skill would know that a memory device needs a block size and address and control information to respond, the claims do not state that such information forms a part of the read request. In fact, the claims do not even require that such information be part of the same request packet. Even though the memory device needs this information, the claims need not recite every component necessary to enable operation of a working device. Rodime PLC v. Seagate Tech., Inc., 174 F.3d 1294, 1303, 50 USPQ2d 1429, 1435 (Fed. Cir. 1999) (applicant need not claim every feature of a working device). The district court's construction would render claim language in dependent claims 27 and 28 meaningless. This court disfavors such a construction. Comark Communications, 156 F.3d at 1187; Wright Med. Tech., Inc. v. Osteonics Corp., 122 F.3d 1440, 1445, 43 USPQ2d 1837, 1841 (Fed. Cir. 1997).

The district court also relied on a statement made during prosecution as an admission by Rambus that a "transaction request" includes "identification information." At the time of this statement, however, pending claim 186 (issued claim 1 of the '918 patent) referred to "a transaction request including identification information." The examiner amended the claim by inserting the word "packet" after each occurrence of "request" in pending claim 186, which in fact clarifies that identification information is part of a request packet, not a "transaction request." Notably, the examiner did not make such amendments to pending claims 200 and 208, which recited "identification information and a read request." See also '804 patent, col. 26, ll. 4-5.

Finally, this court perceives no justification for including multiplexing as a part of the meaning of "read request." Multiplexing, if necessitated by the claims, is applicable to the construction of the term "bus," not "read request." The claims do not support reading multiplexing into "read request."

From the correct perspective of one of skill in the art at the time of invention, the term "read request" means a series of bits used to request a read of data from a memory device where the request identifies what type of read to perform. The terms "write request" and "transaction request" mean, respectively, a series of bits used to request a write of data to a memory device and a series of bits used to request performance of a transaction with a memory device.

C. Bus

The district court construed "bus" to mean "a multiplexed set of signal lines used to transmit address, data and control information." In its Markman opinion, the district court noted Rambus's proposed ordinary meaning of "bus," but held that the patentees acted as their own lexicographer by redefining "bus" to be a multiplexed bus. Multiplexing refers to the sharing of a single set of lines to send multiple types of information. Under the district court's construction, the "bus" carries three types of information: address, data, and control information.

The term "bus" is very common in the electrical arts and has a well-recognized meaning in such arts, namely, a set of signal lines (e.g., copper traces on a circuit board) to which a number of devices are connected, and over which information is transferred between devices. The New IEEE Standard Dictionary of Electrical and Electronic Terms 141 (5th ed. 1993). The claims generally recite outputting data over a "bus." The claims do not specify that the bus multiplexes address, data, and control information. See '918 patent, col. 26, ll. 19-27. Nothing in the claims compels a definition different from the ordinary meaning of "bus." Before according "bus" this meaning, however, this court must consider the usage and meaning of the term as used in the relevant context of the specification.

In general, most references to "bus" in the specification do not limit the ordinary meaning of this term. Only two references potentially limit the meaning of "bus" in the context of the specification. In the Summary of the Invention, the patentee stated that the "present invention" includes a bus for carrying substantially all address, data, and control information. '918 patent, col. 3, ll. 50-60. The patentee further stated that "the bus carries device-select information without the need for separate device-select lines connected directly to individual devices."[6] Id. In the Detailed Description, the patentee stated:

The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices . . . . The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many systems using the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines.

'918 patent, col. 5, ll. 36-46. See also '918 patent, col. 5, ll. 52-53. While clear language characterizing "the present invention" may limit the ordinary meaning of claim terms, see Scimed, 242 F.3d at 1343; Bell Atlantic, 262 F.3d at 1268, such language must be read in context of the entire specification and the prosecution history. Although the above references, taken alone, may suggest some limitation of "bus" to a multiplexing bus, the remainder of the specification and prosecution history shows that Rambus did not clearly disclaim or disavow such claim scope in this case. See Inverness Med. Switz. Gmbh v. Princeton Biomeditech Corp., 309 F.3d 1365, 1372, 64 USPQ2d 1926, 1932 (Fed. Cir. 2002) (statements made during prosecution were not a clear and unambiguous disclaimer of a claim scope). Thus, Rambus did not limit the ordinary meaning of "bus" in the patents-in-suit.

In this case, the prosecution history shows that a multiplexing bus is only one of many inventions disclosed in the '898 application. Although some of Rambus's claimed inventions require a multiplexing bus, multiplexing is not a requirement in all of Rambus's claims. A careful review of the prosecution histories of the patents-in-suit shows that Rambus expressly recited multiplexing in the claim language for claims limiting the bus to the inventive multiplexing bus. For example, original claim 1 of the '898 application recites a "bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said memory device." Other original claims further require that the "bus carry[ ] device-select information without the need for separate device-select lines connected directly to individual semiconductor devices." This claim language indicates that Rambus did not redefine "bus" in the specification to be a multiplexing bus. Indeed, it is because Rambus viewed "bus" under its ordinary meaning that Rambus specified -- in the claim language -- that the inventive multiplexing bus carries substantially all address, data, and control information and that the bus operates without the need for device-select lines.

Several restriction requirements issued by the PTO also clarify that some of the inventions described in the '898 application did not require the multiplexing bus. The PTO issued an eleven-way restriction requirement during prosecution of the '898 application. Later, during prosecution of U.S. Patent No. 5,841,580 (the grandparent of the '918 patent and the parent of the '263 patent), the PTO issued a two-way restriction, dividing the claims into two distinct groups: a multiplexing bus group (Group I) and a latency invention group (Group II). That two-way restriction stated:

[T]he memory device in Group I does not require the access-time register of Group II, and the semiconductor device in Group II does not require the plurality of conductor [sic] being multiplexed to receive an address as claimed in Group I.

Rambus elected to prosecute the latency claims from Group II in the '580 patent. Therefore, the claims of the '580 patent do not require a multiplexing bus. The claims of the '580 patent, however, do recite a "bus." See '580 patent, col. 24., l. 46. By stating that the latency claims, which recited a "bus," do not require multiplexing, the PTO demonstrated an understanding of "bus" that is not limited to a multiplexing bus.

The specification and prosecution histories, taken in their entirety, convince this court that Rambus did not redefine "bus" to be a multiplexing bus in the patents-in-suit. None of Rambus's statements constitute a clear disclaimer or disavowal of claim scope. In these patents, the term "bus" carries its ordinary meaning as a set of signal lines to which a number of devices are connected, and over which information is transferred between devices.

In sum, the district court erred in its construction of each of the disputed terms. In light of the revised claim construction, this court vacates the grant of JMOL of noninfringement and remands for the district court to reconsider infringement.

IV. Fraud

The jury found that Rambus committed actual fraud by not disclosing to JEDEC patents and patent applications related to the SDRAM and DDR-SDRAM standards. The district court denied JMOL on the SDRAM fraud verdict, but granted JMOL of no fraud on the DDR-SDRAM fraud verdict. Rambus appeals the denial of JMOL on the SDRAM verdict, arguing it did not have patents or applications related to the SDRAM standard while at JEDEC. Infineon cross-appeals the grant of JMOL on the DDR-SDRAM verdict, arguing that the court did not give proper deference to the jury verdict.

To prove fraud in Virginia, a party must show by clear and convincing evidence: 1) a false representation (or omission in the face of a duty to disclose), 2) of a material fact, 3) made intentionally and knowingly, 4) with the intent to mislead, 5) with reasonable reliance by the misled party, and 6) resulting in damages to the misled party. ITT Hartford Group, Inc. v. Va. Fin. Assocs., Inc., 520 S.E.2d 355, 361 (Va. 1999); Bank of Montreal v. Signet Bank, 193 F.3d 818, 826 (4th Cir. 1999). A party's silence or withholding of information does not constitute fraud in the absence of a duty to disclose that information.[7] Bank of Montreal, 193 F.3d at 827. Generally, "'fraud must relate to a present or a pre-existing fact, and cannot ordinarily be predicated on unfulfilled promises or statements as to future events.'" Patrick v. Summers, 369 S.E.2d 162, 164 (Va. 1988) (quoting Soble v. Herman, 9 S.E.2d 459, 464 (Va. 1940)); see also ITT Hartford Group, 520 S.E.2d at 361. In some cases, however, misrepresentations about a party's present intentions also may give rise to fraud. Elliott v. Shore Stop, Inc., 384 S.E.2d 752, 756 (Va. 1989). Failure to prove even one of the elements of fraud -- such as existence of a duty to disclose -- defeats a fraud claim. Bank of Montreal, 193 F.3d at 826.

A. Duty to Disclose

Before determining whether Rambus withheld information about patents or applications in the face of a duty to disclose, this court first must ascertain what duty Rambus owed JEDEC. Mr. John Kelly, EIA's general counsel since 1990 and the person responsible for implementing the EIA/JEDEC patent policy, testified that three manuals, namely, EP-3-F, EP-7-A, and JEP 21-I, contain the patent disclosure policy. Before 1993, JEDEC's policy discouraged the adoption of standards that "call for the exclusive use of a patented item or process." The policy also discouraged standards referring to a "patented item or process" unless the committee knew "the technical information covered by the patent" and the patentee agreed to license the patent under reasonable terms.

JEP 21-I, published in October 1993, stated:

EIA and JEDEC standards . . . that require the use of patented items should be considered with great care. . . . [C]omittees should ensure that no program of standardization shall refer to a product on which there is a known patent unless all the relevant technical information covered by the patent is known . . . .

The manual also included a policy revision expressly adding "pending patent[s]" to the policy language. The manual further stated:

The Chairperson . . . must . . . call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking. Appendix E (Legal Guidelines Summary) provides copies of viewgraphs that should be used at the beginning of the meeting to satisfy this requirement.

Appendix E read, in relevant part, as follows :

EIA/JEDEC PATENT POLICY SUMMARY

Standards that call for the use of a patented item or process may not be considered by a JEDEC committee unless all of the relevant technical information covered by the patent or pending patent is known to the committee, subcommittee, or working group.

Appendix E also provided that patentees or applicants must agree to license others to use the patent "for the purpose of implementing the standard(s)." Thus, Appendix E prohibited standards that "call for use of a patented item or process" unless all information "covered by the patent or pending patent" was known and a "license . . . for the purpose of implementing the standard(s)" was available under reasonable terms. Mr. Willibald Meyer, Infineon's JEDEC representative, explained how members learned of the EIA/JEDEC patent policy. He testified:

Q. In your experience in the years you have attended JEDEC, Mr. Meyer, how is it that members learn what the patent policy is? Is it from reading manuals?

A. Very unlikely.

Q. How is it that members of JEDEC learn of the patent policy?

A. Well, you go to the meetings, you attent [sic] a couple of times, and you learn from how the meeting works and how things are dealt with.

Mr. Meyer further testified that the "patent policy" was discussed orally at each JC-42.3 meeting. Mr. Reese Brown, a JEDEC consultant who edited the standards and maintained the activity log for committee JC-42, also testified that he learned of the patent policy from the Appendix E viewgraphs shown at the meetings. He testified:
Q. When you went to the JC-42.3 meetings, did you look up on the wall when they put the patent policy on the wall?
A. Yes, I read it on the screen.
Q. And that's what you understood the patent policy to be?
A. Yes.
Q. And when you look at the minutes, they would have a copy of that patent policy attached to the minutes so in case you were dozing or doodling or typing on your computer, you could read the patent policy if you wanted?
A. One could if they wanted to.
Q. So in any event, that's where you got your understanding of the patent policy?
A. Yes.

According to the written minutes of committee JC-42.3, JEDEC members were shown the "patent policy" as essentially recorded in Appendix E at each of the committee meetings. For example, the minutes of a July 21, 1992 meeting in Denver, Colorado, entitled "EIA/JEDEC Minutes of Meeting No. 63," indicate that members were shown the patent policy as contained in Attachment A to the minutes. Attachment A reads:
EIA Policy

3.4 Patented Items or Processes

Avoid requirements in the EIA Standards that call for use of a patented item or process. No program standard shall refer to a patented item or process unless all of the technical information covered by the patent is known to the formulating committee or working group . . . .

Other committee minutes indicate that this same language was displayed at meetings held in December 1993, in San Diego, California, and again in December 1995, in Dallas, Texas. The record does not indicate that the directive to the chairman was shown to JEDEC members. Instead, the record indicates that the only "patent policy" ever shown members was the policy as recorded in Appendix E.

The language of these policy statements actually does not impose any direct duty on members. While the policy language advises JEDEC as a whole to avoid standards "calling for the use of" a patent and the manual obligates the chairperson to remind members to inform the meeting of any patents or applications relevant to the work of the committee, this court finds no language -- in the membership application or manual excerpts -- expressly requiring members to disclose information. There is no indication that members ever legally agreed to disclose information.

Nevertheless, because JEDEC members treated the language of Appendix E as imposing a disclosure duty, this court likewise treats this language as imposing a

disclosure duty. Assuming such a duty, however, the directive to the chairperson was not intended as a statement of the duty, but as a requirement on the chairperson to point members to the duty in Appendix E. Nothing in this record suggests that the directive to the chairperson is broader than the policy shown to members by the viewgraphs of Appendix E. Only the language of Appendix E was shown to members. Appendix E prohibited standards that "call for use of a patented item or process" and encouraged disclosure of information "covered by the patent or pending patent." It was that language that the chairperson was instructed to show members to inform them of their duty. That language links the disclosure duty to patents or applications whose claims cover the proposed JEDEC standard. Further, the JEDEC policy permitted adoption of a standard covered by a patent if the claimed technology was available under reasonable license terms. Thus, JEDEC's policy identifies the duty to disclose based on the scope of claimed inventions that would cover any standard and cause those who use the standard to infringe.

Although the JEDEC policy does not use the language "related to," the parties consistently agree that the JEDEC policy language requires disclosure of patents "related to" the standardization work of the committee. Infineon, however, argues this language also requires disclosure of patent applications "related to" the committee's work. While both parties repeatedly treat the "related to" language as coextensive with the policy language, the parties differ in their interpretation of "related to." Rambus argues that "related to" means patents that read on or cover the standard. Although advocating a "more is better" interpretation, the necessary implication of Infineon's arguments also is that whether a patent or application is "related to" the standard depends on the claims of the patent or application.

Rambus disclosed the '703 patent in September 1993. JEDEC also learned of Rambus's WIPO application at the same meeting. Infineon argues that the '703 patent disclosed to JEDEC did not "relate to" the SDRAM standard, but that other undisclosed applications did "relate to" the SDRAM standard. Additionally, Mr. Meyer, Infineon's JEDEC representative, testified that he read the '703 patent and the WIPO application and concluded that they did not "relate to" the SDRAM standard. This conclusion is telling because the written description and drawings of the undisclosed patents and applications are identical to the disclosed '703 patent. The only material difference between the disclosed '703 patent and the undisclosed patents and applications appears in the claims. Accepting, as the jury also must have, Infineon's argument that the '703 patent is unrelated to the JEDEC standard but that undisclosed patents and applications (with the same written description and drawings) are related to the standard, whether a patent or application is "related to" the standard necessarily must depend on the claims of the patent or application.

Indeed, other Infineon arguments evince that this interpretation of "related to" is correct. For example, Infineon states that the '703 patent "contained claims relating only to . . . RDRAM" and did not indicate that Rambus might file "applications based on the same specification, but with SDRAM-related claims." Accepting Infineon's arguments, again as the jury must have, the necessary

implication of those arguments is that "related to" -- and thus the disclosure duty -- focuses on the claims.

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